## **LESSON PLAN**

Discipline:	Semester:	Name of the Faculty:
Computer	Third(3 <sup>rd</sup> )	Er Namita Sukla
Science Engg.		
Subject:	No. of days/week	Semester from Date: 15.09.22 to Date: 22.12.22
Computer	class allotted:	No. of Weeks: 15
System	Four(4)	No. of Weeks. 15
Architecture		
Architecture		
WEEK	CLASS DAY	THEORY TOPICS
	1 <sup>st</sup>	Basic Structure of computer hardware
	2 <sup>nd</sup>	Functional Units
st 1	3 <sup>rd</sup>	Cont
	4 <sup>th</sup>	Computer components
	1 <sup>st</sup>	Performance measures
	2 <sup>nd</sup>	Memory addressing Memory Operations
2 <sup>nd</sup>	3 <sup>rd</sup>	Review Class
	4 <sup>th</sup>	Fundamentals to instructions
		Operands
	ct	Op codes
	1 <sup>st</sup>	Instruction formats
	2 <sup>nd</sup>	Cont
3 <sup>rd</sup>	3 <sup>rd</sup>	Cont
	4 <sup>th</sup>	Addressing techniques
4 <sup>th</sup>	1 <sup>st</sup>	Addressing Modes
	2 <sup>nd</sup>	Continue
	3 <sup>rd</sup>	Review Class
	4 <sup>th</sup>	Monthly Test
	1 <sup>st</sup>	Registers files
	2 <sup>nd</sup>	Complete instruction execution
		Fetch

5 <sup>th</sup>	3 <sup>rd</sup>	Decode
5	5	
		Execution
	11	
	4 <sup>th</sup>	Hard wire control
		TIATU WITE COILLIOI
	1 <sup>st</sup>	Cont.
	2 <sup>nd</sup>	
	۷	Microprogrammed control
	ord o	
	3 <sup>rd</sup>	Cont.
6 <sup>th</sup>		3310
٥	4 <sup>th</sup>	Review Class
	1 <sup>st</sup>	Monthly Test
	<del>-</del>	,,
	2 <sup>nd</sup>	Memory characteristics
	۷	Wellioty characteristics
7 <sup>th</sup>	3 <sup>rd</sup>	Memory – hierarchy
/	3	Memory - merarchy
	-th	
	4 <sup>th</sup>	Cont
	1 <sup>st</sup>	Semiconductor RAM organization
	2 <sup>nd</sup>	Semiconductor ROM organization
8 <sup>th</sup>	3 <sup>rd</sup>	Interleaved Memory
	5	interiouved intelliory
	4 <sup>th</sup>	Cooke memory
	4	Cache memory
	1 <sup>st</sup>	
	1	Cont
	_ nd	
	2 <sup>nd</sup>	Virtual memory
+h	l	
9 <sup>th</sup>	3 <sup>rd</sup>	Cont
	4 <sup>th</sup>	Review Class
	_ st	10 H T
	1 <sup>st</sup>	Monthly Test
	2 <sup>nd</sup>	Input-Output interface
	۷	Input-Output Interface
10 <sup>th</sup>	ard	Modes of data two wafers
	3 <sup>rd</sup>	Modes of data transfer
	+h	
	4 <sup>th</sup>	Programmed I/O/Transfer
	1 <sup>st</sup>	Interment driven i/a
		Interrupt driven i/o
	2 <sup>nd</sup>	Cont
	_	
11 <sup>th</sup>	3 <sup>rd</sup>	DMA
	5	DIMI

	_ th	
	4 <sup>th</sup>	Cont
	1 <sup>st</sup>	I/O Channel architecture
12 <sup>th</sup>	2 <sup>nd</sup>	Review Class
	3 <sup>rd</sup>	Bus& system bus
	4 <sup>th</sup>	Types of system Bus – Data bus
13 <sup>th</sup>	1 <sup>st</sup>	Address bus
	2 <sup>nd</sup>	Control Bus
	3 <sup>rd</sup>	Bus Structure
	4 <sup>th</sup>	Basic parameter of Bus Design.
14 <sup>th</sup>	1 <sup>st</sup>	SCSI, USB
	2 <sup>nd</sup>	Review Class
	3 <sup>rd</sup>	Monthly Test
	4 <sup>th</sup>	Parallel Processing
15 <sup>th</sup>	1 <sup>st</sup>	Linear Pipeline
	2 <sup>nd</sup>	Multiprocessor
	3 <sup>rd</sup>	Flynn's Classification
	4 <sup>th</sup>	Review Class